Smart encoders & actuators

User's guide

ASC85

- Singleturn rotary encoder with optical scanning
- Large 50 mm / 1.9685" thru-bore shaft
- Resolution up to 25 bits, high accuracy ±0.005°
- SSI and BiSS C-mode interfaces
- Sine-Cosine 1Vpp additional track
- For direct integration into robots, radars and motors

Suitable for the following models:

- ASC85xx/GG...
- ASC85xx/SC...

Table of Contents

General contents

Subject Index

Typographic and iconographic conventions

In this guide, to make it easier to understand and read the text the following typographic and iconographic conventions are used:

- parameters and objects both of Lika device and interface are coloured in **GREEN**;
- alarms are coloured in **RED**;
- states are coloured in **FUCSIA**.

When scrolling through the text some icons can be found on the side of the page: they are expressly designed to highlight the parts of the text which are of great interest and significance for the user. Sometimes they are used to warn against dangers or potential sources of danger arising from the use of the device. You are advised to follow strictly the instructions given in this guide in order to guarantee the safety of the user and ensure the performance of the device. In this guide the following symbols are used:

	This icon, followed by the word **WARNING**, is meant to highlight the parts of the text where information of great significance for the user can be found: user must pay the greatest attention to them! Instructions must be followed strictly in order to guarantee the safety of the user and a correct use of the device. Failure to heed a warning or comply with instructions could lead to personal injury and/or damage to the unit or other equipment.
	This icon, followed by the word **NOTE**, is meant to highlight the parts of the text where important notes needful for a correct and reliable use of the device can be found. User must pay attention to them! Failure to comply with instructions could cause the equipment to be set wrongly: hence a faulty and improper working of the device could be the consequence.
	This icon is meant to highlight the parts of the text where suggestions useful for making it easier to set the device and optimize performance and reliability can be found. Sometimes this symbol is followed by the word **EXAMPLE** when instructions for setting parameters are accompanied by examples to clarify the explanation.

Preliminary information

This guide is designed to provide the most complete and exhaustive information the operator needs to correctly and safely install and operate the **ASC85 absolute encoders with SSI / BiSS C-mode interface**.

ASC85 is the large thru-bore rotary encoder with high singleturn resolution up to 25 bits and high accuracy ±0.005°. This encoder is able to provide a total amount of position information up to 25 bits (25 bits = 33,554,432 cpr). Thus the overall length of the SSI data packet is up to 25 bits; while the overall length of the BiSS data packet is up to 33 bits (25 bit position information + 1 bit error nE + 1 bit warning nW + 6 bit CRC cyclic redundancy check). It further provides additional 1Vpp sine-cosine signals for speed feedback (4096 sinusoidal waves per mechanical revolution). For information on the encoder resolution please see the order code.

To make it easier to read and understand the text, this guide can be divided into three main sections.

In the first section some general information concerning the safety, the mechanical installation and the electrical connection as well as tips for setting up and running properly and efficiently the unit are provided.
In the second section, entitled **SSI interface**, both general and specific information is given on the SSI interface.
In the third section, entitled **BiSS C-mode interface**, both general and specific information is given on the BiSS C-mode interface. In this section the parameters implemented in the unit are fully described.

1 - Safety summary

1.1 Safety

- Always adhere to the professional safety and accident prevention regulations applicable to your country during device installation and operation;
- installation and maintenance operations have to be carried out by qualified personnel only, with power supply disconnected and stationary mechanical parts;
- device must be used only for the purpose appropriate to its design: use for purposes other than those for which it has been designed could result in serious personal and/or the environment damage;
- high current, voltage and moving mechanical parts can cause serious or fatal injury;
- warning! Do not use in explosive or flammable areas;
- failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment;
- Lika Electronic assumes no liability for the customer's failure to comply with these requirements.

1.2 Electrical safety

- Turn off power supply before connecting the device;
- connect according to explanation in the "4 - Electrical connections" section on page 13;
- if not used, connect Zero setting and Counting direction inputs to 0Vdc;
  - to set the zero, connect Zero setting input to +Vdc for 100 µs at least, then disconnect +Vdc; normally voltage must be at 0Vdc; zero must be set after Counting direction; we suggest setting the zero when the encoder shaft is not running;
  - Counting direction: CW increasing count (viewed from fixing plate side): connect to 0Vdc; CCW increasing count: connect to +Vdc;
- in compliance with the 2014/30/EU norm on electromagnetic compatibility, following precautions must be taken:

  - before handling and installing, discharge electrical charge from your body and tools which may come in touch with the device;
  - power supply must be stabilized without noise, install EMC filters on device power supply if needed;
  - always use shielded cables (twisted pair cables whenever possible);
  - avoid cables runs longer than necessary;
  - avoid running the signal cable near high voltage power cables;
  - mount the device as far as possible from any capacitive or inductive noise source, shield the device from noise source if needed;
  - to guarantee a correct working of the device, avoid using strong magnets on or near by the unit;
  - minimize noise by connecting the shield and/or the connector housing and/or the frame to ground. Make sure that ground is not affected by noise. The connection point to ground can be situated both on the device side and on user's side. The best solution to minimize the interference must be carried out by the user.

1.3 Mechanical safety

- Install the device following strictly the information in the "3 - Mounting instructions" section on page 11;
- mechanical installation has to be carried out with stationary mechanical parts;
- do not disassemble the encoder;
- do not tool the encoder or its shaft;
- delicate electronic equipment: handle with care; do not subject the device and the shaft to knocks or shocks;
- respect the environmental characteristics declared by manufacturer.

2 - Identification

Device can be identified through the **order code** and the **serial number** printed on the label applied to its body. Information is listed in the delivery document too. Please always quote the order code and the serial number when reaching Lika Electronic. For any information on the technical characteristics of the product refer to the technical catalogue.

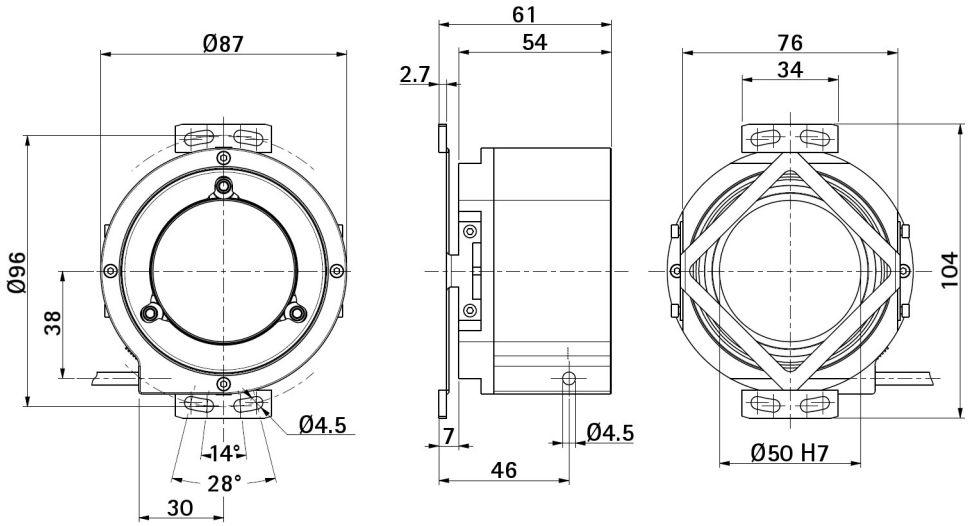
Warning: encoders having order code ending with "/Sxxx" may have mechanical and electrical characteristics different from standard and be supplied with additional documentation for special connections (Technical Info).

3 - Mounting instructions

WARNING
Installation must be carried out by qualified personnel only, with power supply disconnected and mechanical parts compulsorily in stop.

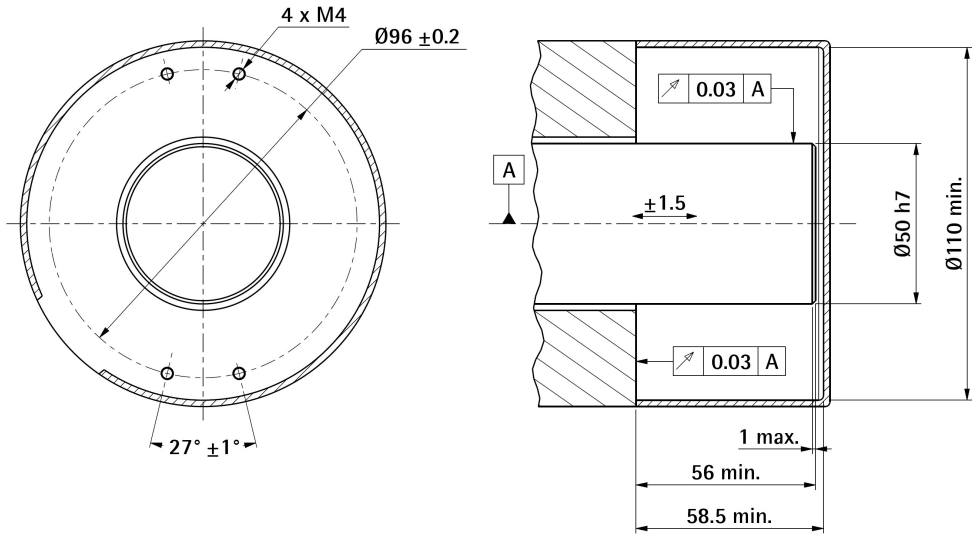
3.1 ASC85 encumbrance sizes

(values are expressed in mm)



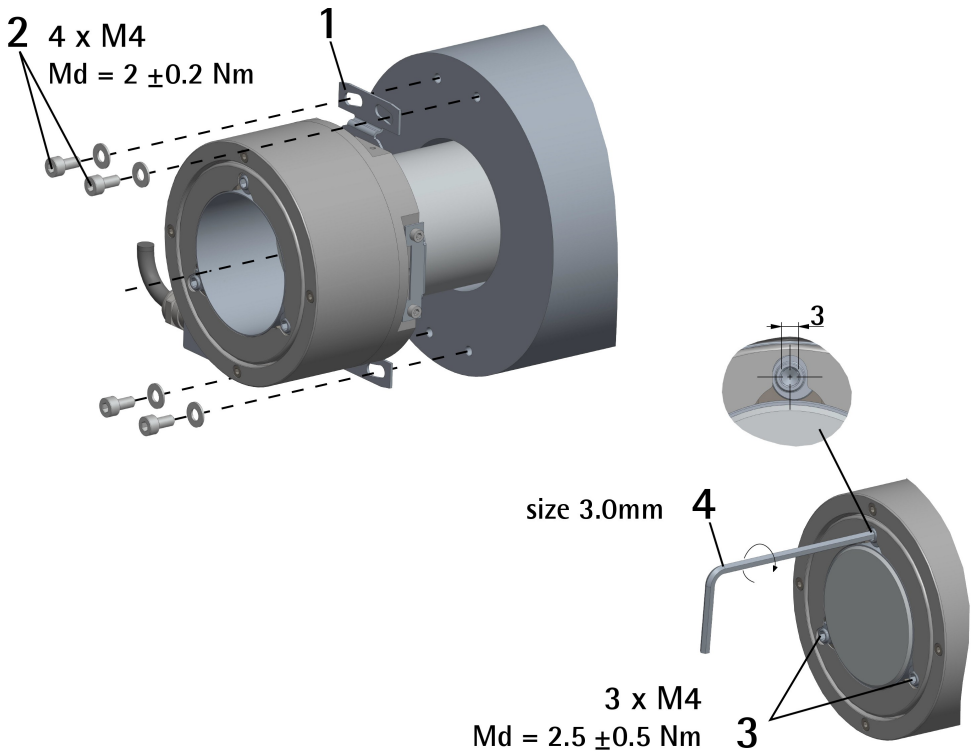
3.2 Mechanical characteristics of the mounting support

(values are expressed in mm)



3.3 Mounting the encoder

- Mount the encoder on the motor shaft. Avoid forcing the encoder shaft;
- fasten the fixing plate **1** to the rear of the motor using four M4 screws with washers **2**; max. tightening torque: 2 ±0.2 Nm;
- fix the encoder shaft by tightening the three M4 eccentric screws **3** by means of a 3.0 mm size hex key **4**. Max. tightening torque: 2.5 ±0.5 Nm.



4 - Electrical connections

WARNING
Power supply must be turned off before performing any electrical connection!
If wires of unused signals come in contact, irreparable damage could be caused to the device. Thus they must be cut at different lengths and insulated singularly.

Function	M23 12-pin	M12 12-pin	TF12 cable
CLOCK IN + / MA +	2	3	Violet
CLOCK IN - / MA -	1	4	Yellow
DATA OUT + / SLO +	3	5	Grey
DATA OUT - / SLO -	4	6	Pink
A (COS +)	5	9	Green
/A (COS -)	6	10	Brown
B (SIN +)	7	11	Red
/B (SIN -)	10	12	Black
Counting direction [1]	8	8	Blue
Zero setting / Preset [1]	9	7	White
0Vdc	12	1	White/Green
+Vdc [2]	11	2	Brown/Green
Shield	Case	Case	Shield

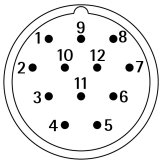
n.c. = not connected

1 Only available for SSI interface (see the order code .../GG...)

2 See the order code for power supply voltage level

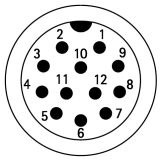
EXAMPLE
ASC85xx/SC**1**-... +Vdc = +5Vdc ± 5%
ASC85xx/SC**2**-... +Vdc = +10Vdc +30Vdc

4.1 M23 12-pin connector



M23 12-pin connector
Counter-clockwise
Male frontal side

4.2 M12 12-pin connector



M12 12-pin connector
Male frontal side

4.3 TF12 cable specifications

Model	: LIKA TF12 encoder cable
Cross section	: 6 x 2 twisted pairs (28 AWG)
Jacket	: special flame retardant PVC compound
Shield	: tinned copper braid, coverage > 80%
Outer diameter	: 5.4 mm ±0.1 mm (0.21" ±0.004")
Min. bending radius	: min. 54 mm (2.12")
Work temperature	: -15°C +80°C (+5°F +176°F)
Conductor resistance	: < 242.02 Ω/km

4.4 GND connection

Minimize noise by connecting the shield and/or the connector housing and/or the frame to ground. Make sure that ground is not affected by noise. The connection point to ground can be situated both on the device side and on user's side. The best solution to minimize the interference must be carried out by the user.

4.5 1Vpp sinusoidal output signals

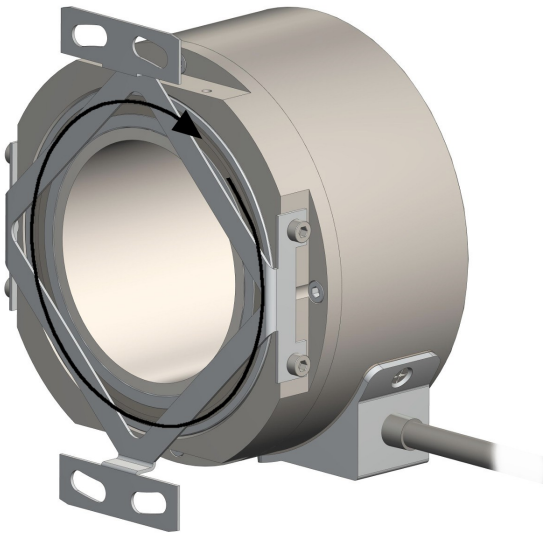
For any further information on the 1Vpp sinusoidal signals please refer to the "7 - 1Vpp sine/cosine output signals" section on page 35.

4.6 Counting direction input

The Counting direction input is available for SSI interface only (see the order code .../GG...).
The Counting direction input allows to set whether the position value output by the encoder increases when the encoder shaft rotates clockwise (CW) or counter-clockwise (CCW). The clockwise rotation is intended as shown in the Figure. If the Counting direction input is connected to 0Vdc, the position value increases when the encoder shaft rotates clockwise; on the contrary, if the Counting direction input is connected to +Vdc, the position value increases when the encoder shaft rotates counter-clockwise. If not used, connect the Counting direction input to 0Vdc (standard counting direction, see the Figure).

WARNING
After changing the counting direction you are required to set a new zero.

NOTE
The counting direction function affects the absolute position information, not the sine/cosine signals.



4.7 Zero setting input

The Zero setting input is available for SSI interface only (see the order code .../GG...).
The output position information at a point in the shaft rotation can be set to 0. The Zero setting input allows the operator to activate the zero setting function by using an input signal sent by a PLC or other controller. To activate the zero setting function, connect the Zero setting input to +Vdc for 100 µs at least, then disconnect +Vdc; normally voltage must be at 0Vdc. Zero setting must be set after Counting direction. We suggest setting the zero setting function when the encoder shaft is not running. If not used, connect the Zero setting input to 0Vdc.

5 - SSI interface

Order code: ASC85xx/GG...

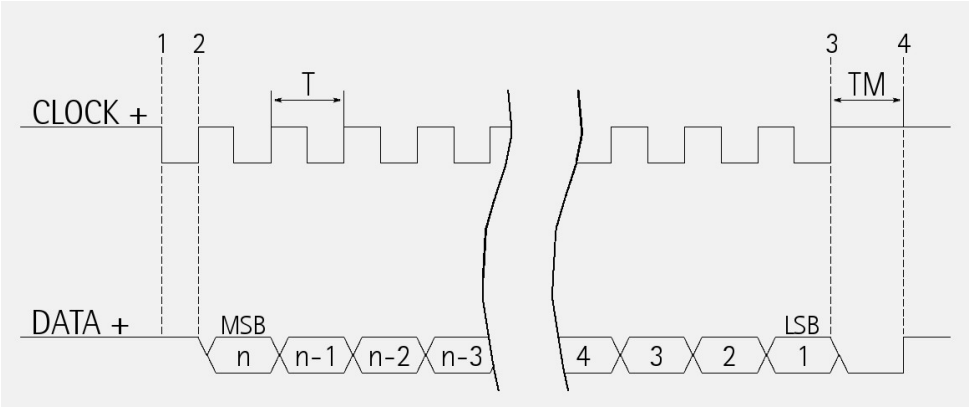
5.1 SSI (Synchronous Serial Interface)

SSI (the acronym for **Synchronous Serial Interface**) is a synchronous point-to-point serial interface engineered for unidirectional data transmission between one Master and one Slave. Developed in the first eighties, it is based on the RS-422 serial standard. Its most peculiar feature is that data transmission is achieved by synchronizing both the Master and the Slave devices to a common clock signal generated by the controller; in this way the output information is clocked out at each controller's request. Furthermore only two pairs of twisted wires are used for data and clock signals, thus a six-wire cable is required.
The main advantages in comparison with parallel or asynchronous data transmissions are:

- less conductors are required for transmission;
- less electronic components;
- possibility of insulting the circuits galvanically by means of optocouplers;
- high data transmission frequency;
- hardware interface independent from the resolution of the absolute encoder.

Furthermore the differential transmission increases the noise immunity and decreases the noise emissions. It allows multiplexing from several encoders, thus process controls are more reliable with simplified line design and easier data management.

Data transmission is carried out as follows.
At the first falling edge of the clock signal (**1**, the logic level changes from high to low) the absolute position value is stored while at the following rising edge (**2**) the transmission of data information begins starting from the MSB.



At each change of the clock signal and at each subsequent rising edge (**2**) one bit is clocked out at a time, up to LSB, so completing the data word transmission. The cycle ends at the last rising edge of the clock signal (**3**). This means that up to n + 1 rising edges of the clock signals are required for each data word transmission (where n is the bit resolution); for instance, a 13-bit encoder needs 14 clock edges. If the number of clocks is greater than the number of bits of the data word, then the system will send a zero (low logic level signal) at each additional clock, zeros will either lead (LSB ALIGNED protocol) or follow (MSB ALIGNED protocol) or lead and/or follow (TREE FORMAT protocol) the data word. After the period Tm monoflop time, having a typical duration of 12 µsec, calculated from the end of the clock signal transmission, the encoder is then ready for the next transmission and therefore the data signal is switched high.
The clock signal has a typical logic level of 5V, the same as the output signal which has customarily a logic level of 5V in compliance with RS-422 standard.
The output code is Gray (see the order code).

5.2 "MSB left aligned" protocol

"MSB left aligned" protocol allows to left align the bits, beginning from MSB (most significant bit) to LSB (least significant bit); MSB is then sent at the first clock cycle. If the number of clock signals is higher than the data bits, then unused bits are forced to logic level low (0) and follow the data word. This protocol can be used in encoders having any resolution.
The number of clocks to be sent to the encoder must equal the number of data bits at least, anyway it can be higher, as stated previously. The great advantage of this protocol over the TREE format or the LSB RIGHT ALIGNED format is that data can be transmitted with a minimum time loss and Tm monoflop time can immediately follow the data bits without any additional clock signal.
The length of the word is variable according to the resolution, as shown in the following table.

Model	Length of the word	Max. number of information
ASC8520/...	20 bits	1,048,576
ASC8521/...	21 bits	2,097,152
ASC8522/...	22 bits	4,194,304
ASC8523/...	23 bits	8,388,608
ASC8524/...	24 bits	16,777,216
ASC8525/...	25 bits	33,554,432

The output code is GRAY (see the order code).

Structure of the position information

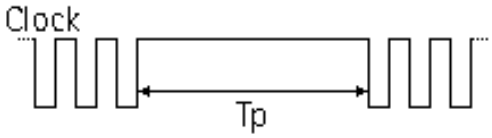
ASC8520/...	**bit**	**19**	**...**	**0**
	...			
ASC8525/...	**bit**	**24**	**...**	**0**
	value	MSB	...	LSB

5.3 Recommended transmission rates

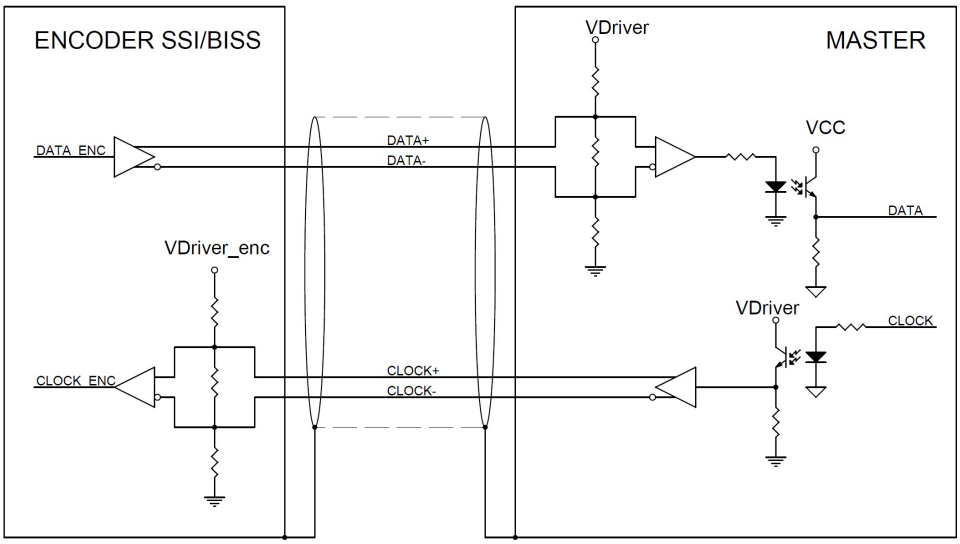
The SSI interface has a frequency of data transmission ranging between 100 kHz and 4 MHz.
CLOCK IN and DATA OUT signals comply with the "EIA standard RS-422".
The SSI clock frequency (baud rate) depends on the length of the cable and must comply with the technical information reported in the following table:

Cable length	Baud rate
< 50 m	< 400 kHz
< 100 m	< 300 kHz
< 200 m	< 200 kHz
< 400 m	< 100 kHz

The time interval between two Clock sequence transmissions must be at least 12 µs (Tp > 12 µs).



5.4 Recommended SSI input circuit



6 - BiSS C-mode interface

Order code: ASC85xx/SC...

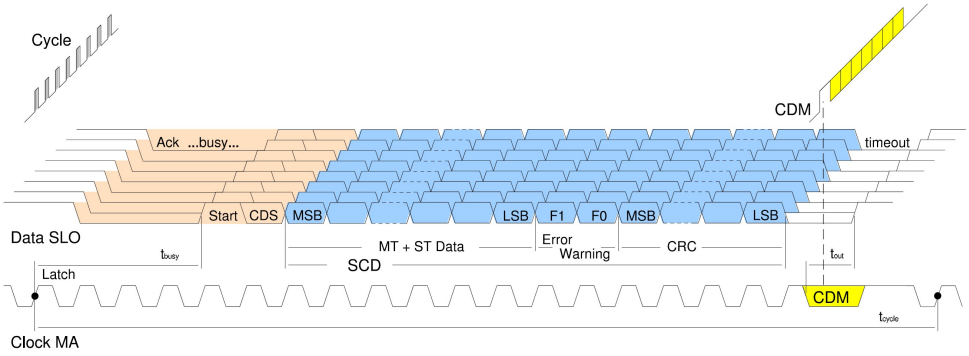
Lika encoders are always Slave devices and comply with the "BiSS C-mode interface" and the "Standard encoder profile".
Refer to the official BiSS website for all information not listed in this manual (www.biss-interface.com).
The device is designed to work in a point-to-point configuration and has to be installed in a "single Master, single Slave" network.
CLOCK IN (MA) and DATA OUT (SLO) signal levels are according to the "EIA standard RS-422".

WARNING
Never install the encoder in a "single Master, multi Slave" network.

6.1 Communication

The BiSS C-mode protocol uses two types of data transmission protocols:

- **Single Cycle Data (SCD):** it is the main data transmission protocol. It is used to send process data from the Slave to the Master. For any information refer to the "6.2 Single Cycle Data SCD" section on page 21.
- **Control Data (CD):** transmission of a single bit following the SCD data. It is used to read or write data into the registers of the Slave. For any information refer to the "6.3 Control Data CD" section on page 22.



6.2 Single Cycle Data SCD

6.2.1 SCD structure

SCD data has a variable length according to the resolution of the encoder. It is nbitres+8 long where "nbitres" is the resolution of the encoder expressed in bits. It consists of the following elements: position value (**Position**), 1 error bit nE (**Error**), 1 warning bit nW (**Warning**) and a 6-bit CRC Cyclic Redundancy Check (**CRC**).

bit	nbitres+7 ... 8	7	6	5 ... 0
function	Position	Error	Warning	CRC

Position
(Nbitres)
It is the process data transmitted from the Slave to the Master. It has a variable length, it is as long as the resolution of the encoder expressed in bits.
It provides information about the current position of the encoder.
The transmission starts with msb (most significant bit) and ends with lsb (least significant bit). "Nbitres" is the resolution of the encoder expressed in bits.

bit	nbitres+7	...	...	8
value	msb	...	...	lsb

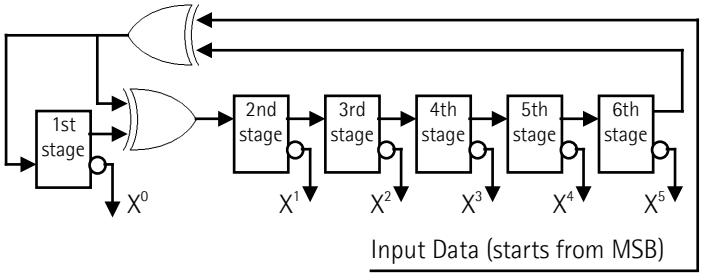
See also the register **Position** on page 30.

Error
(1 bit)
It is intended to communicate the normal or fault status of the Slave.
When nE = "0" (low active), an error is active in the system. For a comprehensive list of the available error messages and their meaning please refer to the register 69 **Error register** on page 31 ff.
nE = "1": no active error
= "0": error status: an error is active in the system.

Warning
(1 bit)
It is intended to communicate the normal or fault status of the Slave.
When nW = "0" (low active), a warning is active in the system. For a comprehensive list of the available warning messages and their meaning please refer to the register 69 **Error register** on page 31 ff.
nW = "1": no active warning
= "0": warning status: a warning is active in the system.

CRC
(6 bits)
Correct transmission control (inverted output). Cyclic Redundancy Check is an error checking which is the result of a "Redundancy Checking" calculation performed on the message contents. This is intended to check whether transmission has been performed properly. It is 6-bit long.
Polynomial: X^6+X^1+1 (binary: 1000011)

Logic circuit



6.3 Control Data CD

Main control data is described in this section. Please refer to the official BiSS documents for complete CD structure: "BiSS C Protocol Description" in the BiSS homepage.

Register address
It sets the number of the register you need either to read or to write. It is 7-bit long.

RW
RW = "01": when you need to write in the register.
RW = "10": when you need to read in the register.
It is 2-bit long.

DATA
When you need to write in a register (**RW** = "01"), it allows to enter the value to be written in the register (transmitted from the Master to the Slave).
When you need to read in a register (**RW** = "10"), it shows the value read in the register (transmitted from the Slave to the Master).
It is 8-bit long.

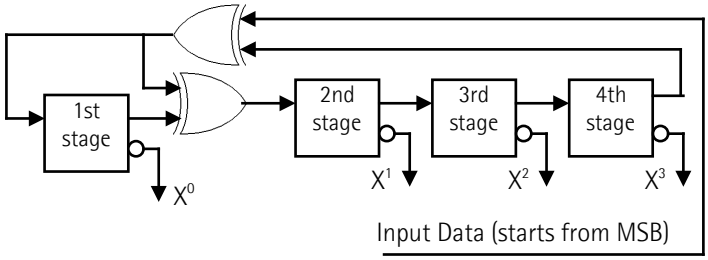
Data bit structure:

bit	7	...	...	0
	msb	...	...	lsb

CRC

Correct transmission control (inverted output). Cyclic Redundancy Check is an error checking which is the result of a "Redundancy Checking" calculation performed on the message contents. This is intended to check whether transmission has been performed properly. It is 4-bit long.
Polynomial: X^4+X^1+1 (binary: 10011)

Logic circuit:



6.4 Implemented registers

Register (hex)	Function
40	Bank selection
42 - 43	Profile ID
44 ... 47	Serial number
5A	Diagnostic data
60	Command & status
61 ... 64	Position
69	Error register
78 ... 7D	Device ID
7E - 7F	Manufacturer ID

All registers described in this section are listed as follows:

Function name
[Address, Attribute]
Description of the function and specification of the default value.

- Address: the register address is expressed in hexadecimal notation.
- Attribute: ro = read only
  rw = read and write
  wo = write only
- Default parameter value is written in **bold**.

Bank selection

[40, rw]

ASC85 encoder is equipped with an internal EEPROM that offers the user 1kbit additional storage space for user data.
The EEPROM is organized in 4 memory banks.
Banks 0 and 1 are reserved and not available to user.
Banks 2 and 3 provides 64 byte free memory space each one. 64 registers are addressed from 00h to 3Fh in each bank and can be used to store personal data.
The **Bank selection** register is used to switch to the additional memory banks 2 and 3 on the internal EEPROM.
The value of the **Bank selection** register is not saved in non-volatile memory. After each power-on its value will be 0h and banks 0-1 will be automatically selected.

Value of the register	Bank	Availability
0h	Bank 0	Reserved use
1h	Bank 1	
2h	Bank 2	Additional storage space available to user
3h	Bank 3	

Profile ID

[42 - 43, ro]

These registers contain the identification code of the used profile.
The used encoder profile is **BP1: Standard Encoder Profile**. Default value for the Profile ID is:

Register	42	43
	MSB	LSB
	28	19
	Singleturn resolution, Variant 0-24++	Data length = 25 bits (see on page 21)

See "Standard encoder profile", "data format", "Variant 0-24".

Serial number

[44 ... 47, ro]

These registers contain the serial number of the device in ascending order expressed in hexadecimal notation.

Serial number registers structure:

Register	44	45	46	47
	Serial number			
	MSB	...	...	LSB
	2^{31} ... 2^{24}	2^{23} ... 2^{16}	2^{15} ... 2^{8}	2^{7} ... 2^{0}

EXAMPLE

Serial number 171256846 dec is expressed as shown in the table:

Register	44	45	46	47
	0A	35	2C	0E

Diagnostic data

[5A, ro]

This register offers diagnostic information and specifies the kind of problem signalled through bit 0 **Control error** or bit 1 **Signal error** in the register 69 **Error register**. The high logic level (= 1) shows the active error.

Register	5A							
	msb							lsb
bit	7	6	5	4	3	2	1	0

Bit 0

AC minimum amplitude

This error is active simultaneously with the bit 1 **Signal error** in the register 69 **Error register**.

The signal monitoring circuit verifies that differential signals show an acceptable AC amplitude. As soon as the lower differential voltage threshold (minimum amplitude of the signals) is detected, the error bit is set to 1.

Bit 1

DC minimum offset

This error is active simultaneously with the bit 1 **Signal error** in the register 69 **Error register**.

The signal monitoring circuit verifies that all analogue signal lines show an acceptable DC voltage. As soon as the minimum voltage threshold (minimum offset) is detected, the error bit is set to 1.

Bit 2

Signal level minimum amplitude

This error is active simultaneously with the bit 0 **Control error** in the register 69 **Error register**.
The signal level monitoring circuit has detected the lower threshold (minimum amplitude). The error bit is set to 1.

Bit 3

Amplitude control minimum current

This error is active simultaneously with the bit 0 **Control error** in the register 69 **Error register**.
The monitoring circuit of the Amplitude Control output current has detected the lower threshold (minimum current). The error bit is set to 1.

Bit 4

AC maximum amplitude

This error is active simultaneously with the bit 1 **Signal error** in the register 69 **Error register**.
The signal monitoring circuit verifies that differential signals show an acceptable AC amplitude. As soon as the upper differential voltage threshold (maximum amplitude of the signals) is detected, the error bit is set to 1.

Bit 5

DC maximum offset

This error is active simultaneously with the bit 1 **Signal error** in the register 69 **Error register**.
The signal monitoring circuit verifies that all analogue signal lines show an acceptable DC voltage. As soon as the maximum voltage threshold (maximum offset) is detected, the error bit is set to 1.

Bit 6

Signal level maximum amplitude

This error is active simultaneously with the bit 0 **Control error** in the register 69 **Error register**.
The signal level monitoring circuit has detected the upper threshold (maximum amplitude). The error bit is set to 1.

Bit 7

Amplitude control maximum current

This error is active simultaneously with the bit 0 **Control error** in the register 69 **Error register**.
The monitoring circuit of the Amplitude Control output current has detected the upper threshold (maximum current). The error bit is set to 1.

Command & status

[60, rw]

This register can be accessed either in write mode or in read mode and changes its function depending on the type of access. If you access the register in a write mode, it acts as a **command register** (Command mode). If you access the register in a read mode, it returns the **current system status** (Status mode).

Command mode

[wo]

If you access the register 60 **Command & status** in a write mode, it acts as a command register. The available commands are listed in the following table.

Command	Function
00	Request of new position data
01	Write current configuration to EEPROM
02	Read new data via absolute data interface
03	Trigger software reset
04	Verify CRC of internal configuration
05	Error simulation: activate Error message status
06	Error simulation: delete Error message status

Request of new position data

If **command 00** is written, new position data is requested. As long as the new data is not available, the bit 0 **Position data valid** in the **Status mode** of the **Command & status** register is set to 0 = FALSE. Position data can be read in the registers 61-64 **Position**.

Write current configuration to EEPROM

Command 01 allows to write (i.e. to save) the current configuration to the EEPROM. Configuration registers from 00h up to 2Dh (they are reserved for use to Lika Electronic engineers and not available to users) plus a newly generated check sum are written.

For the whole duration of the writing process the status bit 3 **Internal data bus busy** in the **Status mode** of the **Command & status** register is set to 1 = TRUE. Furthermore the **Error register** indicates the **Configuration error** (bit 4 = 1 = ACTIVE ERROR). If an error occurs during writing, the bit 4 **Configuration error** is not reset at the end of the process.
If no EEPROM is connected up at switching on, command 01 has no effect.

Read new data via absolute data interface

Command 02 triggers a new reading of absolute data by the absolute data interface. If the execution is successful, the cycle counter is set; otherwise it will be set to zero. The status bit 2 **Absolute data valid** in the **Status mode** of the **Command & status** register and the error bit 6 **Absolute data error** in the **Error register** are set accordingly.

Trigger software reset

Command 03 initiates a software reset. The system accesses the EEPROM to source its CRC-protected configuration data. If the configuration data is not confirmed by its CRC at first attempt (for example when an EEPROM is connected up that has not been programmed yet), all configuration registers are set to zero, the error bit 4 **Configuration error** in the **Error register** is set to 1 and the serial I/O interface is activated with the SSI protocol. If there is no EEPROM, the internal registers are set to zero, the error bit 4 **Configuration error** in the **Error register** is set to 1 and the interface is activated according to settings.

Verify CRC of internal configuration

Command 04 triggers a CRC of the internal configuration. During this operation, all configuration registers are reviewed and verified by the check sum. During this process, the status bit 3 **Internal data bus busy** in the **Status mode** of the **Command & status** register is set to 1 = TRUE. Furthermore the **Error register** indicates the **Configuration error** (bit 4 = 1 = ACTIVE ERROR). If an error occurs, the bit 4 **Configuration error** is not reset at the end of the process.

Error simulation: activate Error message status

Command 05 and **Command 06** simulate an error status to be signalled through the bit 6 **Error message** in the **Status mode** of the **Command & status** register.
Command 05 allows to force high (1 = TRUE) the bit 6 **Error message**.

Error simulation: delete Error message status

Command 05 and **Command 06** simulate an error status to be signalled through the bit 6 Error message in the **Status mode** of the Command & status register.
Command 06 allows to force low (0 = FALSE) the bit 6 Error message.

Status mode
[ro]

If you access the register 60 Command & status in a read mode, it returns the current system status. The logic level LOW (=0) indicates that the status is FALSE; the logic level HIGH (=1) indicates that the status is TRUE.

Register	60							
	msb							lsb
bit	7	6	5	4	3	2	1	0

Bit 0
Position data valid

When this bit has logic level high 1 = TRUE, it signals that the current position data is valid. Refer also to the command 00 **Request of new position data** on page 27.

Bit 1
Absolute data valid

When this bit has logic level high 1 = TRUE, it indicates that absolute data has been loaded successfully through the absolute data interface. Data is accepted only if the CRC is correct and the error bit is inactive. Refer also to the command 02 **Read new data via absolute data interface** on page 28.

Bit 2
Internal data bus busy

When this bit has logic level high 1 = TRUE, it indicates that the internal data bus is busy, for example during CRC verification or when configuration data is being read out from or written to the EEPROM. Refer also to the command 01 **Write current configuration to EEPROM** on page 27; and to the command 04 **Verify CRC of internal configuration** on page 28.

Bit 3

Write access permitted to EDS memory area

When this bit has logic level high 1 = TRUE, it indicates that a write access is permitted to EDS (Electronic Data Sheet) memory area (otherwise, if the value is 0 = FALSE, a write protection is active).

Bit 4

Write access permitted to CONF memory area

When this bit has logic level high 1 = TRUE, it indicates that a write access is permitted to CONF (Configuration Data) memory area (otherwise, if the value is 0 = FALSE, a write protection is active).

Bit 5

Warning message

When this bit has logic level high 1 = TRUE, it indicates that a warning message is currently active. For detailed information on the active warning refer to the register 69 Error register on page 31.

Bit 6

Error message

When this bit has logic level high 1 = TRUE, it indicates that an error message is currently active. For detailed information on the active error refer to the register 69 Error register on page 31.

Bit 7

Configuration completed

When this bit has logic level high 1 = TRUE, it indicates that the configuration registers have been successfully CRC verified and the absolute data has been correctly read by the absolute data interface.

Position

[61-64, ro]

Registers 61-64 contain the absolute position information.

Position registers structure:

Register	61	62	63	64
	LSB	...	...	MSB
	2^7 and 2^6 (2^5 ... 2^0 = not used)	2^{15} ... 2^8	2^{23} ... 2^{16}	2^{31} ... 2^{24}

Error register

[69, ro]

This register is meant to show the warning and error messages that are currently active (the relevant bit = "1") in the encoder. The fault condition is also signalled through the bit 5 **Warning message** and/or the bit 6 **Error message** in the **Status mode** of the **Command & status** register. Please note that, after resetting the message (the reset is performed upon reading out position data), if the problem that caused the message to be triggered has not been solved, the warning or error message will be invoked to appear again.

Register	69							
	msb							lsb
bit	7	6	5	4	3	2	1	0

Bit 0

Control error

When this bit has logic level high 1 = ACTIVE ERROR, it indicates that a control error is currently active. For more detailed information on the kind of error, refer to bit 2 **Signal level minimum amplitude**, bit 3 **Amplitude control minimum current**, bit 6 **Signal level maximum amplitude** and bit 7 **Amplitude control maximum current** in the register 5A **Diagnostic data** (see on page 25).

Bit 1

Signal error

When this bit has logic level high 1 = ACTIVE ERROR, it indicates that a signal error is currently active. For more detailed information on the kind of error, refer to bit 0 **AC minimum amplitude**, bit 1 **DC minimum offset**, bit 4 **AC maximum amplitude** and bit 5 **DC maximum offset** in the register 5A **Diagnostic data** (see on page 25).

Bit 2

Not used

Bit 3

Synchronization error

When this bit has logic level high 1 = ACTIVE ERROR, it indicates that a failure occurred in the internal synchronization between the cycle counter and the interpolator.

Bit 4

Configuration error

When this bit has logic level high 1 = ACTIVE ERROR, it indicates that a configuration error is currently active. It may be triggered because of one of the following reasons:

- switching on without EEPROM;
- CRC error at switching on with EEPROM;
- write error after write access to the EEPROM following the command 01 **Write current configuration to EEPROM** in the **Command mode** of the Command & status register (see on page 27);
- temporarily during write access to the EEPROM following the command 01 **Write current configuration to EEPROM** in the **Command mode** of the Command & status register (see on page 27);
- CRC error after a software reset following the command 03 **Trigger software reset** in the **Command mode** of the Command & status register (see on page 28);
- CRC error after CRC verification following the command 04 **Verify CRC of internal configuration** in the **Command mode** of the Command & status register (see on page 28);
- temporarily during CRC verification following the command 04 **Verify CRC of internal configuration** in the **Command mode** of the Command & status register (see on page 28);
- failure in the EEPROM.

Bit 5

Interpolation error

When this bit has logic level high 1 = ACTIVE ERROR, it indicates that the conversion has not been carried out at time of read access.

Bit 6

Absolute data error

When this bit has logic level high 1 = ACTIVE ERROR, it indicates that an absolute data interface error is currently active. It may be triggered because of one of the following reasons:

- the absolute data interface received BiSS data containing a CRC error;
- the absolute data interface received BiSS data with error bit nE (**Error**) low active (0).

NOTE

Please note that the **Absolute data error** bit is kept at 0 if the absolute data interface is not configured.

Bit 7
Not used.

Device ID

[78 ... 7D, ro]
These registers contain the Device ID (name and hardware-software release). Identification name is expressed in hexadecimal ASCII code.
Registers 78 ... 7B show the name of the device.
Registers 7C and 7D show the hardware-software release.
Device ID **registers structure:**

Register	78	79	7A	7B	7C	7D
	2^{47} ... 2^{40}	2^{39} ... 2^{32}	2^{31} ... 2^{24}	2^{23} ... 2^{16}	2^{15} ... 2^{8}	2^{7} ... 2^{0}
Hex	**41**	**53**	**38**	**35**	**31**	**31**
ASCII	**A**	**S**	**8**	**5**	**1**	**1**

Manufacturer ID

[7E – 7F, ro]
These registers contain the Manufacturer ID. Identification name is expressed in hexadecimal ASCII code.
Manufacturer ID **registers structure:**

Register	7E	7F
	2^{15} ... 2^{8}	2^{7} ... 2^{0}
Hex	**4C**	**69**
ASCII	**L**	**i**

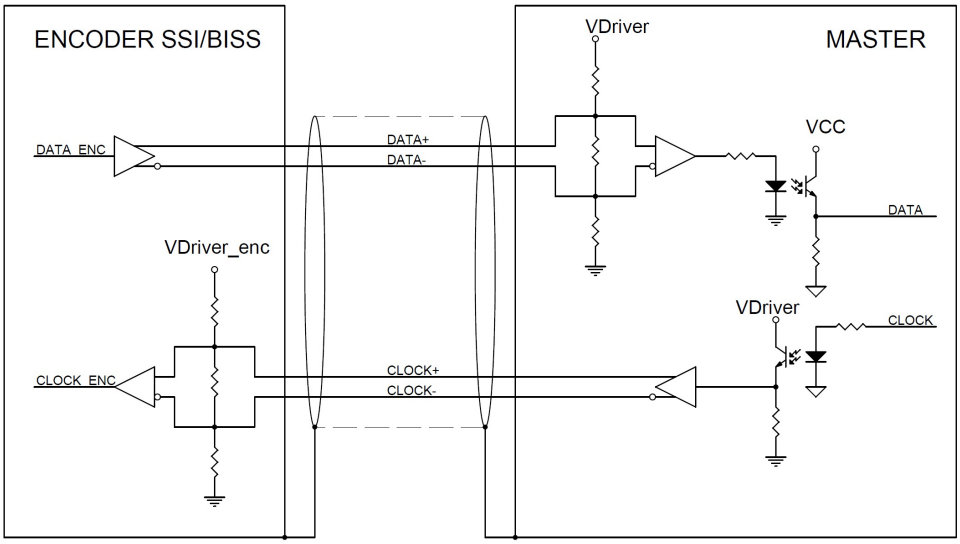
Li = Lika Electronic

6.5 Application notes

Data transmission:

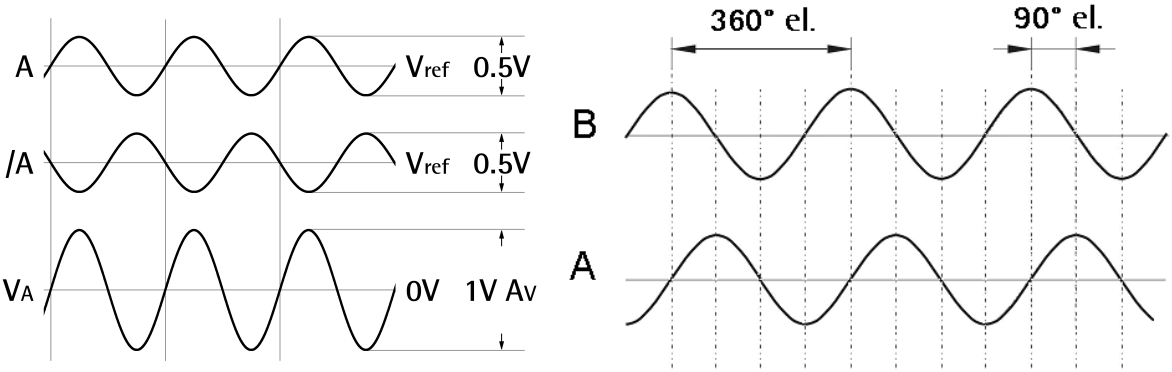
Parameter	Value
Clock Frequency	min 100KHz, max 10MHz
BiSS time-out	adaptive (typ. 0.35 µs @ 10 MHz)

6.6 Recommended BiSS input circuit



7 - 1Vpp sine/cosine output signals

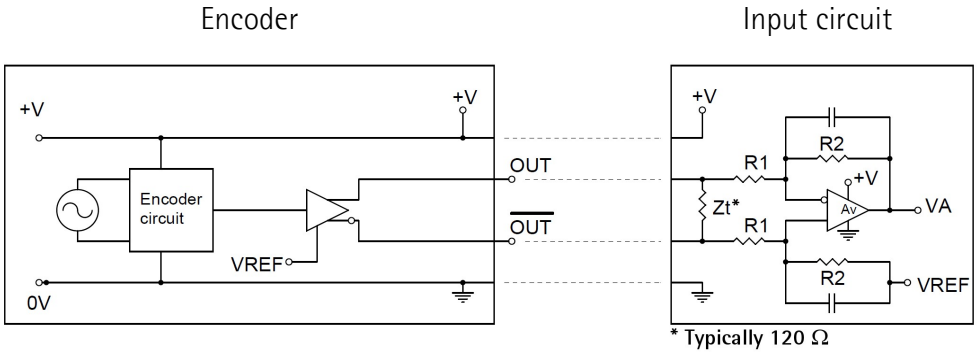
A (COSINE) and B (SINE) signals are to be intended with CW rotation as viewed in the Figure in the "4.6 Counting direction input" section on page 14. They provide 4096 sinusoidal waves per mechanical revolution with amplitude 1Vpp. 1Vpp output level results from differential signals detection. The frequency of output signals is proportional to the rotational speed of the encoder.



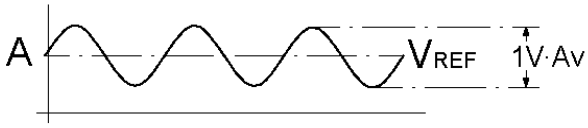
7.1 Output signals voltage level

The voltage level refers to the differential value between normal and inverted signal (differential).

Recommended input circuit



V_{REF} = 2.5V ± 0.5V V_A = 1Vpp * Av Av = R2 / R1



Document release	Release date	Description	HW	SW	Interface
1.0	19.05.2017	First issue	0	1	-
1.1	16.03.2018	SCD data structure of BiSS modified	1	1	-
1.2	01.06.2018	M12 12-pin connector instead of M12 8-pin. Counting direction and Zero setting inputs added to SSI interface	1	1	-
1.3	06.07.2018	Section "4 - Electrical connections" updated	1	1	-
1.4	12.11.2018	Bank selection register added. Sine-Cosine additional track information added	1	1	-

This device is to be supplied by a Class 2 Circuit or Low-Voltage Limited Energy or Energy Source not exceeding 30 Vdc. Refer to the order code for supply voltage rate.
Ce dispositif doit être alimenté par un circuit de Classe 2 ou à très basse tension ou bien en appliquant une tension maxi de 30Vcc. Voir le code de commande pour la tension d'alimentation.

Dispose separately

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